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| 09/493,319 | 01/28/2000 | Samson Huang | INTL-0312-US (P7995) | 2102 |

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| ART UNIT | PAPER NUMBER |
|---|---|
| 2675 | 11 |

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/493,319 | HUANG, SAMSON | |
| | Examiner | Art Unit | |
| | Leland R. Jorgensen | 2675 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19, 21 - 26, 28 - 32, 40, 41, 43, and 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19, 21 - 26, 28 - 32, 40, 41, 43, and 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Specification*

1. In view of the amendment filed 25 March 2003, the objection to the title is withdrawn.

### *Drawings*

2. In view of the amendment filed 25 March 2003, the objection to the drawings is withdrawn.

### *Claim Objections*

3. In view of the amendment filed 25 March 2003, the objections to now cancelled claims 20, 27, 34, and 42 are withdrawn.

### *Claim Rejections - 35 USC § 112*

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 19 and 21 – 25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the office action of 18 December 2002, examiner rejected claims 19 – 44 because the claims described a first memory and a second memory. The specifications describe only a memory 66. In response, applicant amended the claims and argued

"The claims have also been amended to recite one memory, thereby overcoming the § 112, first paragraph rejections of claims 19-44." Claim 19, however, still describes a "a first memory local to the pixel cell ... to store a digital indication of a predetermined voltage;" and "a memory to store a digital indication of the predetermined voltage." As written, this suggests that there are two memories: a first memory and a memory. Claim 20 further suggests that the memory is different from the first memory. Claim 20 is dependant on claim 19 and adds that "the memory is local to the pixel cell." Claim 19 already established that the first memory is local to the pixel cell.

6. Claims 19 and 21 – 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As noted above, claim 19 describes a first memory and a memory. It is unclear whether the first memory and the memory are the same or different.

Claims 19 and 21 – 25 are also rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 19 – 25 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in Paper No. 10 filed 25 March 2003. In that paper, applicant has stated "The claims have also been amended to recite one memory, thereby overcoming the § 112, first paragraph rejections of claims 19-44.", and this statement indicates that the invention is different from what is defined in the claim(s) because claim 19 seems to teach two memories, a first memory and a memory. See discussion above about the 35 U.S.C. 112, first paragraph, rejection for further details.

*Claim Rejections - 35 USC § 102*

7. Claims 19, 21 - 23, 25, 26, 28, 30, 31, 40, 41, and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakajima, USPN 6,333,737 B1.

**Claims 19, 26, and 40**

Nakajima teaches a pixel 2 for a liquid crystal display. Nakajima, figures 1 and 2; col. 2, lines 44 – 47; and col. 3, lines 11 – 17. Nakajima teaches providing a storage capacitor for each pixel. Nakajima, col. 1, lines 13 – 21; col. 2, line 67 – col. 3, line 5; col. 3, lines 22 – 25; and figure 1. Nakajima teaches a first memory [memory 22] for each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1a.

Nakajima teaches a digital to analog conversion circuit 25 at each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1. Although Nakajima does not specifically describe converting the digital indication into an analog voltage during a refresh operation, it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

**Claims 21, 28**

Nakajima teaches that the first memory 22 is local to the pixel cell. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1a.

**Claims 22, 30, 44**

Nakajima teaches that the memory may be a RAM. Nakajima, col. 3, lines 57 – 59.

**Claim 23**

Nakajima adds the step of reading the digital indication from the memory. Nakajima, col. 3, line 66 – col. 4, line 4; and col. 5, lines 51 – 52. Nakajima does not specifically describe

the reading during the refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

**Claim 25, 41**

It is inherent to the operation of Nakajima that the refresh operation occurs at a different rate than the frame update operation. Nakajima specifically teaches,

> Further, if each pixel is provided with the output means for outputting data for displaying pixels (display data) on the basis of the processed data in addition to the operating means, the operational processing can be immediately performed on the data input to a pixel from the external or adjacent pixels to display the pixel concerned.

Nakajima, col. 2, lines 14 – 20. See also: Nakajima, col. 5, lines 17 – 26; col. 5, line 42 – col. 6, line 3.

***Claim Rejections - 35 USC § 103***

8. Claims 24, 29, 32, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Kinoshita et al, USPN 5,771,031.

**Claims 24, 32**

Claims 24 and 32 each add the step of latching the digital indication from the memory during the refresh operation. As understood in the art, latching is holding data in a circuit until other circuits are ready to change the latch circuit.

Nakajima does not specifically teach the step of latching the information from the memory.

Kinoshita teaches the step of latching the information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method and circuits as taught by Nakajima with the latching method and circuit taught by Kinoshita. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display. Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 – 21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9. Kinoshita invites such combination by teaching,

> In the trend of resent years, the number of pixels in each horizontal pixel array is increased to improve the resolution of the active matrix LCD, and the word length of each pixel data is also increased to improve the precision of the gray scale. In order to increase the number of pixels and the word length, it is necessary for the signal line driving circuit to process the pixel data at a higher speed. However, if the processing speed of the signal line driving circuit is improved to its limit, it is difficult to drive all the signal lines within one horizontal scanning period.

Kinoshita, col. 1, lines 28 – 37. Kinoshita adds as the object of invention,

> An object of the present invention is to provide a flat-panel display device and a method of driving the same, which can maintain the memory capacity required for block-driving of each horizontal pixel array to be small.

Kinoshita, col. 2, lines 6 – 9. Kinoshita further adds,

> According to the aforementioned flat-panel display device and its driving method, pixel data items sequentially supplied from outside are divided into pixel-data blocks each consisting of the same number of pixel data items, equivalent to

> the number of pixels forming one pixel block. M pixel-data blocks are sequentially written in M memory sections, and the M pixel-data blocks stored in the M memory sections are read in parallel while writing is performed. These M pixel-data blocks are supplied to corresponding ones of the data supply buses. Therefore, the total memory capacity of the memory sections is smaller than a memory capacity required for storing all items of pixel data for one horizontal pixel array. Further, the memory capacity of the memory section is not significantly depend on the number of pixel data items for one horizontal array and the word length of pixel data. This enables an increase in the number of pixel data items for one horizontal pixel array and an increase in the word length while maintaining the memory capacity of the memory section to be small. As a result of this, it is possible to prevent costs for manufacturing a flat-panel display device from being increased due to block driving of the horizontal pixel array.

Kinoshita, col. 2, line 63 – col. 3, line 17. Kinoshita teaches that the memory can be reduced with its latching circuit. Kinoshita, col. 9, lines 59 – 67; and col. 10, lines 60 – 67.

**Claims 29, 43**

Kinoshita teaches that the capacitors are associated with a row of pixels. Kinoshita, col. 4, lines 19 – 22, lines 35 – col. 36, and lines 62 - 65.

***Response to Arguments***

9. Applicant's arguments filed 25 March 2003 have been fully considered but they are not persuasive.

As to claims 19 and 21 – 25, applicant argues that Nakajima neither teaches nor suggests that the memory 22 is local to a pixel cell relative to other pixel cells. In fact, Nakajima specifically teaches such throughout its abstract, specification, and claims. For example,

> In each pixel 2, various image processing such as conversion of the pixel number, decoding of compressed signals, improvement in image quality, etc. can be performed by the operating function which can perform various operational processing. Further, since the input register circuit 21, the memory 22, the operating circuit 23, the output register circuit 24, the DAC circuit 25, etc. are provided in the same pixel 2, so that data input to each pixel 2 can be

> instantaneously subjected to operational processing to obtain a digital signal and then the digital signal is converted to an analog signal to display information of the analog signal on the pixel 2.

Nakajima, col. 6, lines 13 – 24. See also: Nakajima, col 3, lines 11 – 17; col. 5, lines 10 – 16; and figure 1. Nakajima, claim 25, teaches,

> 25. A display device comprising:
>
> a plurality of pixels, each pixel of said plurality of pixels include:
>
> a input register circuit:
>
> memory connected to said input register circuit;
>
> an operating circuit having an operating unit which reads data from said memory, and a register circuit connected to a control line;
>
> an output register connected to said operating circuit; and
>
> a digital-to-analog circuit connected to said output register.

Nakajima, col. 10, lines 4 – 16.

As to claims 26 and 28 – 32, applicant argues that Nakajima neither teaches nor suggests providing memory buffers that are closer to associated pixel cell than to other pixel cells. As Nakajima teaches in the specifications, claims, and figure 1, each pixel has an adjacent circuit including a memory 22. It is inherent that the adjacent circuit be closer to its associated pixel cell than to other pixel cells.

As to claims 40, 43, and 44, applicant argues that Nakajima neither teaches nor suggests spatially distributing memory buffers among pixel cells. Spatial means "relating to, occupying, or having the character of space." Merriam-Webster's Collegiate Dictionary, 10th ed., 1999, p. 1127. As noted above, the plurality of pixels, each with its own memory 22, have memory buffers spatially distributed among the pixel cells.

***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Quanrud, USPN 6,339,417 B1, teaches a display having multiple memory elements per pixel.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

STEVEN SARAS
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TECHNOLOGY CENTER 2600